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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,881	09/28/2005	Stefan Marco Koch	853663.412USPC	8855

38106 7590 03/02/2010

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ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
03/02/2010	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/521,881
Filing Date: September 28, 2005
Appellant(s): KOCH ET AL.

Timothy L. Boller
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 16 November 2009 appealing from the Office action mailed 26 November 2008.

(1) Real Party in Interest

The statement identifying by name of the real party in interest contained in the brief appears to be correct.

2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

Koch et al. (U.S. Pre-grant Publication No. 2002/0055979), published 9 May 2002 - hereinafter "Koch".

Tang et al. (U.S. Patent No. 6,775,717), published 10 August 2004 - hereinafter "Tang".

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Examiner's Note: The amendment filed 26 May 2009 and entered on 15 April 2009 was entered to simplify the issues for appeal. Reflecting the amended claims, the status of the rejections has changed. However, the grounds of rejection remain the same as presented in the Final Action mailed 26 November 2008. As such the Grounds of Rejection to be Reviewed on Appeal identified beyond number 2 (on page 5 of the brief) is the correct one. In hindsight the examiner realizes it may have made the state

of the case more clear if the applicant had instead been advised to cancel the independent claim 13 and rewrite the dependent claims in independent form, so that the status of all relevant claims would have remained the same.

Claims 1-7, 9, 10 and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koch in view of Tang.

As per claim 1, Koch teaches a first processor bus as **[a first processor bus 40 (paragraph 0050 and figure 4)]**, a first processor on a first clock connected to the first processor bus as **[a first processor P1 is connected to a processor bus 40 (paragraph 0050 and figure 4) the first processor P1 on its own clock domain, P1 clock (paragraphs 0046 and 0056)]**, a first direct memory access unit with an external direct memory access channel, and connected to the first processor bus as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4)]**, a first programmable unit **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4)]** comprising a first processor interface coupled, via the first external direct memory access channel, to the first direct memory access unit, said first programmable unit being programmable by the first processor via the first processor interface as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can**

comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)], a first shareable unit being connectable to the first processor bus as **[shareable unit 43 connected to processor bus 40 (figure 4)]**, a second processor bus as **[the second processor bus 50 (paragraph 0050 and figure 4)]**, a second processor on a second clock connected to the second processor bus as **[a second processor P2 that also has a processor bus 50 (paragraph 0050 and figure 4) the second processor P2 on its own clock domain, P2 clock (paragraphs 0046 and 0056)]**, a second direct memory access unit with an external direct memory access channel, and connected to the second processor bus as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4)]**, a second programmable unit **[access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4)]** comprising a second processor interface, the second programmable unit coupled, via the second external direct memory access channel, to the second direct memory access unit, the second programmable unit being programmable by the second processor via the second processor interface as **[access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]** and a second shareable unit being connectable to the second processor bus as **[shareable unit 53 connected to**

the processor bus 50 (figure 4)], wherein the first programmable unit and the second programmable unit each comprise a processor interface, and a direct access unit core as **[the access unit comprises a processor interface, a direct access unit (DAU), and external DMA channel interface (paragraph 0045 and figure 3)]** and wherein a first bi-directional communication channel is established between the first shareable unit and the second processor via the first programmable unit, and a second bi-directional communication channel is established between the second shareable unit and the first processor via the second programmable unit as **[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051), access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) and access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4), which can each be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045)]**.

Koch does not explicitly teach wherein the first programmable unit and the second programmable unit each comprise two external direct memory access channel interfaces, however.

Tang teaches wherein the first programmable unit and the second programmable unit each comprise two external direct memory access channel interfaces as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA channel interface providing a DMA channel request for a next DMA transfer**

(column 2, lines 42-55), connected from the DMAs to the access units taught by Koch, above (such as connecting DMA2 54 to access unit 51 and DMA1 41 to access unit 48 of Koch's figure 4)].

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces. As Koch teaches that the DMA channels are on the same clock as the associated processor and bus to which it is connected, and where the access units decouple the cross-processor dataflow from the clock domain of the incoming processor, so that each of an access(programmable) unit's external channels will be on separate clocks (this is caused by the decoupling, so that the dataflow going toward each processor is on the clock of that respective processor bus) (Koch, paragraphs 0046, 0056, etc.).

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)]**.

As per claim 2, Koch teaches wherein the first and/or second bi-directional channels are half-duplex channels or full-duplex channels as **[the access unit 48 provides a half-duplex channel to and from the processor bus 40 and the DMA unit 54 (paragraph 0055)]**.

As per claim 3, Koch teaches wherein both processors are similar from an architectural point of view as **[processors P1 and P2 are similar from an architectural point of view (claim 2)]**.

As per claim 4, Koch teaches wherein the processors are implementations of the same type of processor design as **[processors P1 and P2 are implementations of the same type of processor design (claim 3)]**.

As per claim 5, Koch teaches wherein the processors are implementations of different types of processor design as **[processors P1 and P2 are implementations of different types of processor design (claim 4)]**.

As per claim 6, Koch teaches wherein the shareable unit is a memory, a peripheral, an interface, an input device or an output device as **[examples of shareable units are: volatile memory, non-volatile memory, peripherals, interfaces, input devices, output devices, and so forth (paragraph 0044)]**.

As per claim 7, Koch teaches wherein one of the two processors is a CPU, a microprocessor, a DSP, a system controller, a co-processor or an auxiliary processor as **[the processors described can be any of the following: a CPU, a microprocessor, a DSP, a system controller, a co-processor, an auxiliary processor, and so forth (paragraph 0043)]**.

As per claim 9, Koch teaches wherein the processor interface has a programming link for either connecting to a corresponding processor bus or for connecting to a corresponding processor as **[the access unit has a data link 33 and a control link 34 for connection to the processor bus (paragraph 0045 and figure 3)]**.

As per claim 10, Koch teaches wherein the first and second bi-directional communication channels transfer data and/or control information to and from the first and second shareable units via the communication channels as **[each communication channel is employed for transferring data and/or control information to and from the shareable units (claim 11)]**.

As per claim 13, Koch teaches a first processor and a first shareable unit coupled to a first bus, the first processor and first shareable unit operating on a first processor clock as **[a first processor P1 is connected to a processor bus 40 (paragraph 0050 and figure 4) the first processor P1 on its own clock domain, P1 clock**

(paragraphs 0046 and 0056) and access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]; a second processor and a second shareable unit coupled to a second bus, the second processor and second shareable unit operating on a second processor clock as **[a second processor P2 that also has a processor bus 50 (paragraph 0050 and figure 4) the second processor P2 on its own clock domain, P2 clock (paragraphs 0046 and 0056) and access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**; a first bi-directional channel to couple the second processor to the first shareable unit via the first and second busses, the first bi-directional channel configured to decouple the clock domain of the second processor from the clock domain of the first shareable unit as **[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051)]**, the first bi-directional channel also coupled through a first programming interface to the second processor as

[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051), where enhanced processor interfaces are provided for linking the processors to the common bus (paragraph 0010)]; wherein the first bi-directional channel comprises a first internal channel of a first DMA unit coupled to the first bus, the first DMA unit configured with a first external channel to operate on the first processor clock as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)]**; a first internal channel of a second DMA unit coupled to the second bus, the second DMA unit configured with a first external channel to operate on the second processor clock as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)]**; and a second bi-directional channel to couple the first processor to the second shareable unit via the first and second busses, the second bi-directional channel configured to decouple the clock domain of the first processor from the clock domain of the second shareable unit as **[a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051), where an access unit decouples the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)]**,

the second bi-directional channel also coupled through a second programming interface to the first processor, the second bi-directional channel being simultaneously operable with the first bi-directional channel between the first and second bus as **[each processor can access, via communication channels, the shareable unit and devices within the processing environment of the other processor without having to go through that processor (paragraphs 0051-0052)]**, wherein the second bi-directional channel comprises an external channel of the first DMA unit to operate on the first processor clock as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)]**; an external channel of the second DMA unit to operate on the second processor clock as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)]**; and a second programmable unit coupled between an external channel of the first DMA unit and an external channel of the second DMA unit as **[access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**.

While Koch teaches that each DMA may also contain a second external channel (see Koch, paragraph 0043), it does not explicitly teach wherein such a second external channel is contained within a second bi-directional channel between the two processors (i.e. connecting the same pair of processors as the first bi-directional channel).

Tang teaches wherein each DMA unit comprises two external channel interfaces (which can connect toward the same direction) as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA channel interface providing a DMA channel request for a next DMA transfer (column 2, lines 42-55)]**.

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces. As Koch teaches that the DMA channels are on the same clock as the associated processor and bus to which it is connected, and where the access units decouple the cross-processor dataflow from the clock domain of the incoming processor, so that each of a DMA unit's external channels will be on the same clocks (the clock is later changed/decoupled by the access unit to change it to the clock of the other DMA/processor) (Koch, paragraphs 0046, 0056, etc.).

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the**

second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)].

As per claim 14, Koch teaches a first programmable unit coupled between the first external channel of the first DMA unit and the first external channel of the second DMA unit as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**, the first programmable unit comprising the first programming interface to the second processor, the first programmable unit also configured to decouple the second processor clock from the first processor clock as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045), where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048) and where the access units 48 and 51 decouple the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)]**.

As per claim 15, Koch teaches a second programmable unit coupled between an external channel of the first DMA unit and an external channel of the second DMA unit as **[access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**, the second programmable unit comprising the second programming interface to the first processor, the second programmable unit also configured to decouple the second processor clock from the first processor clock as **[access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) which can be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) where the access units can comprise their own processor interface, which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048) and where the access units 48 and 51 decouple the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)]**.

As per claim 16, Koch teaches a first external channel of a common programmable unit, the first external channel operating on the second processor clock, and the first external channel also coupled to the first external channel of the second DMA unit and a second external channel of the common programmable unit, the second

external channel to operate on the first processor clock, and the second external channel also coupled to the first external channel of the first DMA unit as **[access unit 51, connected to DMA 41 via its external interface 42 (paragraph 0051 and figure 4) and access unit 48, connected to DMA 54 via its external interface 55 (paragraph 0051 and figure 4) (where the two access units form the common programmable unit), which can each be set up by external agents (such as the processor) for the remote processor to gain access to the shareable unit (paragraph 0045) and where the access units 48 and 51 decouple the data flow between the clock domain of the first processor and the clock domain of the second processor (paragraph 0056)]**; and a first programmable core of the common programmable unit, the first programmable core to operate on the second processor clock as **[the clock signal of processor P2, P2 clock, is fed via clock line 73 to processor interface 72 of access unit 51 (paragraph 0056)]**, the first programmable core coupled between the first and second external channels of the common programmable unit and the first programmable core comprising the first programming interface to the second processor as **[access unit 51 is connected to processor P2 via processor interface 72 (paragraph 0056) which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**.

While Koch teaches that each DMA may also contain a second external channel (see Koch, paragraph 0043), it does not explicitly teach wherein such a second external channel is contained within a second bi-directional channel between the two processors (i.e. connecting the same pair of processors as the first bi-directional channel).

Tang teaches wherein each DMA unit comprises two external channel interfaces (which can connect toward the same direction) as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA channel interface providing a DMA channel request for a next DMA transfer (column 2, lines 42-55)]**.

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces. As Koch teaches that the DMA channels are on the same clock as the associated processor and bus to which it is connected, and where the access units decouple the cross-processor dataflow from the clock domain of the incoming processor, so that each of a DMA unit's external channels will be on the same clocks (the clock is later changed/decoupled by the access unit to change it to the clock of the other DMA/processor) (Koch, paragraphs 0046, 0056, etc.).

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)]**.

As per claim 17, Koch teaches an external channel of the common programmable unit, the external channel to operate on the second processor clock, and the external channel also coupled to the other external channel of the second DMA unit as **[DMA 54, with external interface 55, is connected to the processor bus 50 via interface 57 (paragraph 0052 and figure 4) associated with the second processor clock domain, P2 clock (paragraphs 0046 and 0056)]**; an external channel of the common programmable unit, the external channel to operate on the first processor clock, and the external channel also coupled to the second external channel of the first DMA unit as **[DMA 41, with external interface 42, is connected to processor bus 40 via interface 44 (paragraph 0051 and figure 4) associated with the first processor clock domain, P1 clock (paragraphs 0046 and 0056)]**; and a second programmable core of the common programmable unit, the second programmable core to operate on the first processor clock as **[the clock signal of the first processor P1 (P1 clock) is fed via a clock line 74 to the DAU core 61 and the processor interface 62 of the access unit 48 (paragraph 0056)]**, the second programmable core coupled between the third and fourth external channels of the common programmable unit and the second programmable core comprising the second programming interface to the first processor as **[access unit 48 is connected to processor P1 via processor interface 62 (paragraph 0056) which is adapted to the actual processor and/or processor bus (paragraphs 0045 and 0048)]**.

While Koch teaches that each DMA may also contain a second external channel (see Koch, paragraph 0043), it does not explicitly teach wherein such a second external

channel is contained within the second bi-directional channel between the two processors (i.e. connecting the same pair of processors as the first bi-directional channel).

Tang teaches wherein each DMA unit comprises two external channel interfaces (which can connect toward the same direction) as **[a first DMA channel interface for participating in a first DMA transfer, and a second DMA channel interface providing a DMA channel request for a next DMA transfer (column 2, lines 42-55)]**.

Koch and Tang are analogous art, as they are within the same field of endeavor, namely instruction processing, and DMA control.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces. As Koch teaches that the DMA channels are on the same clock as the associated processor and bus to which it is connected, and where the access units decouple the cross-processor dataflow from the clock domain of the incoming processor, so that each of a DMA unit's external channels will be on the same clocks (the clock is later changed/decoupled by the access unit to change it to the clock of the other DMA/processor) (Koch, paragraphs 0046, 0056, etc.).

The motivation for doing so, as provided by Tang, would have been **[the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the**

second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55)].

As per claim 18, Koch teaches wherein the first bi-directional channel further comprises a first master configured to initiate data transfers with active devices on the first or second busses as **[a system controller is used to initiate transfers over the buses (paragraph 0063)]**.

As per claim 19, Koch teaches wherein the second bi-directional channel further comprises a second master configured to initiate data transfers with active devices on the first or second busses as **[a system controller is used to initiate transfers over the buses (paragraph 0063)]**.

(10) Response to Argument

Regarding arguments "A"

As noted above, the entered after-final amendments to the claims render these arguments moot.

Regarding arguments "B"

In response to applicant's arguments against the references individually (on pages 12-13 of the brief), one cannot show nonobviousness by attacking references

individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appellant argues (on pages 12-14 of the brief) that the combination of the cited references does not suggest two programmable units, each of which has two external direct memory access channel interfaces, each on one of two clocks.

However, as described in the rejection, Koch teaches (with reference to figure 4 of Koch) connecting two processors via DMA1 41, through access (i.e. programmable) unit 51 and DMA2 through access (i.e. programmable unit) 48. Koch further teaches that processor P1 and DMA1 are on clock P1, while processor P2 and DMA2 are on a separate clock domain, clock P2, where access units 48 and 51 serve to decouple the dataflow from one processor from the clock of the other processor (paragraphs 0046 and 0056, etc.).

This means that P2, DMA2, and channels 55 and 58 are on one clock domain (P2), while P1, DMA1 and channels 42 and 58 are on another clock domain (P1). It would be obvious, in light of the setup of the system of Koch, that when adding the second external channel to each DMA, as taught by Tang (which would connect DMA2 to access unit 51, and DMA1 to access unit 48, in figure 4 of Koch) that these two channels would also be on the clock domain of their respective processors (i.e. the connection between DMA2 and unit 51 would be on clock P2, and the connection between DMA1 and unit 48 would be on clock P1). This would also mean that the

access/programmable units each have two external channels, each on its own clock domain, as the access/programmable units are serving to decouple the clock domains from one another (see Koch, paragraphs 0046 and 0056). For example, the connection between unit DMA2 and access unit 51 would be on clock P2 while the connection (numbered 42) between access unit 51 and DMA1 would be on clock P1. Rather than a "further modification", as argued by the appellant (page 14 of the brief), this reasoning is based on maintaining the setup taught by Koch. The examiner contends that it would rather require "further modification" of the combination of Koch and Tang to *not* arrive at this setup.

As a further note, the claims do not explicitly require that the first and second processor clocks are different, though they have been assumed so for the sake of advancing prosecution.

Regarding arguments "C"

Appellant also argues that there is no teaching of the "bidirectional channel further comprises a first programmable unit coupled between the first external channel of a first DMA unit and the first external channel of the second DMA unit" (on pages 15-16 of the brief) or a "second programmable unit coupled between the second external channel of the first DMA and the second external channel of a first DMA and the second external channel of the second DMA" (on page 17 of the brief).

However, as described above regarding arguments "B", in the system taught by Koch there exist two channels between processors P1 and P2 (through DMAs 41 and

54 and access/programmable units 48 and 51). The combination of Koch with Tang suggests a second external channel from each DMA (which would connect DMA2 to access unit 51, and DMA1 to access unit 48, in figure 4 of Koch). This would create several bi-directional channels between processors P1 and P2, each flowing through the DMAs 41 and 54 and access/programmable units 48 and 51 (e.g., besides the original channels shown by Koch, dataflow could go from P1, through bus 40, to DMA1, then to access unit 51, then to DMA2 over the new connection, to bus 50 and there to P2; or from P2 through bus 50 to DMA2, then to access unit 48, then to DMA1 over the new connection, to bus 40 and there to P1), to provide greater access between the processors and for the further reasons provided by Tang, above.

As a further note, the claims do not explicitly require that the first and second bi-directional channels not be the same bi-directional channel, or similarly with the DMAs, etc., though they have been assumed to be different for the sake of advancing prosecution.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/George D Giroux/

Examiner, Art Unit 2183

Conferees:

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117